In The Claims:

1. (original) A structure of non-volatile memory, comprising:

a substrate;

a plurality of bit lines formed in the substrate along a first direction, wherein each of the bit lines also serve as a source/drain (S/D) region;

a first dielectric layer, disposed over the substrate;

a plurality of selection gate (SG) lines formed over the first dielectric layer between the bit lines;

a plurality of charge-storage structure layer, formed over the substrate between the bit lines and the SG lines;

a second dielectric layer, formed over the SG lines;

a third dielectric layer, formed over the bit lines; and

a plurality of word lines, formed over the substrate along a second direction, which is crossing the first direction for the bit lines.

2. (original) The structure of non-volatile memory of claim 1, wherein the charge-storage structure layer includes a charge-trapping dielectric layer.

3. (original) The structure of non-volatile memory of claim 2, wherein the charge-trapping dielectric layer at the region above the bit lines is discontinuous or continuous.

4. (original) The structure of non-volatile memory of claim 2, wherein the charge-trapping dielectric layer includes a horizontal part over the substrate and a vertical part over sidewall of the SG lines.

5. (original) The structure of nonvolatile memory of claim 4, wherein the charge-trapping dielectric layer further comprises another horizontal part over the second dielectric layer.

6. (original) The structure of non-volatile memory of claim 1, wherein the charge-storage structure layers includes a floating gate layer for charge storage.

7. (original) The structure of non-volatile memory of claim 1, further comprising:

a plurality of bank-select transistors respectively disposed between the S/D regions and the bit line voltages for selection and applying the bit line voltage.

8. (original) The structure of non-volatile memory of claim 1, further comprising a source voltage supplying structure coupled to the SG lines, so that a desired voltage state is applied to the selected one of the memory cells to form an operation path.

9. (original) A structure of a non-volatile memory unit with two-bit memory capacity, comprising:

a substrate;

two doped lines, located in the substrate;

a selection gate structure line, disposed on the substrate between the two doped lines;

a charged storage structure layer, located each side of the selection gate structure line between the doped lines and the selection gate line;

a first dielectric layer, disposed over the selection gate structure line;

a second dielectric layer, disposed over the doped lines; and

a gate electrode layer, disposed crossing over the doped lines and the selection gate structure line.

10. (original) The structure of claim 9, wherein the charged storage structure layer comprises a dielectric/charge-storage/dielectric structure layer or a floating gate structure layer.

11. (original) The structure of claim 10, wherein the charged storage structure layer comprises an oxide/nitride/oxide structure layer.

Claims 12-22 (canceled)

No new matter has been added to the application by the amendments made to the claims.

Respectfully submitted,
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